REMARKS

The above Amendments and these Remarks are submitted under 35 U.S.C. § 132 and 37 C.F.R. § 1.111 in response to the Office Action mailed June 9, 2004.

Summary of the Examiner's Action and Applicants' Response

Claims 6 and 10 have been objected to because of informalities. The Examiner rejected Claims 1-11 based on 35 U.S.C. §112. The Examiner has stated that Claim 7 would be allowable if converted to independent form including amendments to overcome the corresponding rejections for its corresponding intervening claims based on 35 U.S.C. §112. The Examiner has objected to the Declaration. Claims 1 and 8-11 have been rejected by the Examiner under 35 U.S.C. 103(a) as being obvious based on Baker, et al., U.S. Patent No. 5,793,954. The Examiner has rejected Claims 2-6 under 35 U.S.C. 103(a) as being obvious based on Baker, et al. in view of Sager, U.S. Patent No. 5,966,544. In response, Applicants submit a new Declaration herewith. In this Amendment, Claims 1, 2, 3, 5, 6, 7, 8, and 10 have been amended. Claims 1-11 remain pending.

Response to Objection to the Declaration

The Examiner states that the declaration does not properly identify the foreign application on which priority is claimed. In response, a new declaration is attached and submitted herewith. Applicants respectfully request, therefore, that the objection to the Declaration be withdrawn.

Response to Objection to Claims 6 and 10

The Examiner has also objected to the language in Claims 6 and 10 as having informalities. Regarding Claim 6, the Examiner stated that the semicolon in Claim 6 needs to be replaced with a colon. The Examiner stated that "even it" in line 3 of Claim 10 is indefinite. In response, Applicants have amended Claims 6 and 10. Applicants respectfully request, therefore, that the objections to Claims 6 and 10 be withdrawn.

Response to Objection to Claim 7

The Examiner has stated that Claim 7 would be allowable if converted to independent form including amendments to overcome the rejections for its corresponding intervening claims

based on 35 U.S.C. §112. In response, Claim 7 has been converted into independent form including amendments to its intervening claims to overcome the corresponding rejections under 35 U.S.C. §112. Applicants respectfully submit that Claim 7 has been placed into allowable form and requests that the objection to Claim 7 be withdrawn.

Response to Rejection of Claims 1-11 under 35 U.S.C. § 112

The Examiner has rejected Claims 1-11 under 35 U.S.C. § 112, second paragraph, because of various informalities. In response, Applicants have amended Claims 1, 2, 3, 5, 6, 8, and 10. Applicants respectfully submit that the rejections to Claims 1-11 under 35 U.S.C. § 112 have been overcome.

Response to Rejection of Claims 1 and 8-11 under 35 U.S.C. §103(a)

Claims 1 and 8-11 have been rejected by the Examiner under 35 U.S.C. 103(a) as being obvious based on Baker, et al. The Examiner states that Baker, et al. discloses a device that has a memory for storing software and is useful for parsing a datastream under program control. The Examiner also states that Baker, et al. does not explicitly teach an "interchangeable program", as claimed in Claim 1. The Examiner contends, however, that Baker, et al. teaches a device that is "programmably configurable" and that this is an obvious variation of an "interchangeable program", as claimed in Claim 1. Applicants respectfully disagree.

In this response, Applicants have amended Claim 1 to more clearly differentiate Baker, et al. More specifically, Applicants have amended Claim 1 to include the "a multiplexable data stream delayline for receiving a data stream" element from Claim 2, as previously amended. Regarding the "multiplexable data stream delayline" element, the Examiner states that, although Baker, et al. does not disclose a multiplexable data stream delayline, Sager teaches this element. Applicants respectfully disagree.

Applicants respectfully submit that Sager teaches a microprocessor having "a replay architecture with an execution core for performing data speculation in executing an instruction, a delay unit for making a copy of the instruction and holding the copy for as long as the instruction takes to execute, and a checker for determining whether the data speculation was bogus". (See Col. 3, lines 53-59). Sager describes "data speculation" as being wherein the processor guesses what values data will have in an attempt to speed up processing. (See Col. 3, lines 13-28). Sager

further teaches that if the "data speculation" was bogus, the delay unit and its buffer will send the copy of the instruction back to the execution core for re-execution. (See Col. 3, lines 59-2). Sager discloses "[a] multiplexor coupled to the input of the execution core **selects for execution among** original instructions from the instruction cache, replay instructions from the delay unit, and manufactured instructions from various other units such as the TLB or tag units, according to a priority scheme." (See Col. 3, lines 54-67, emphasis added). Applicants respectfully submit that Sager does not multiplex a delay line as claimed in Claim 1. In contrast, Sager discloses a multiplexor that selects instructions for execution from among various units according to a priority scheme, the delay line being only one of those units. Sager does not teach or suggest multiplexing within the delay line as claimed in Claim 1. Consequently, the data speculatable processor architecture taught in Sager is not properly combinable with the network analysis device taught in Baker, et al. and even if it were, it would not teach or suggest the device claimed in Claim 1.

Moreover, Sager teaches that the delay unit is for making a **copy** of the instruction and holding **the copy** for as long as the instruction takes to execute. (See Col. 3, lines 53-59). More specifically, Sager discloses a replay architecture which includes a checker unit which receives the output of the hit/miss logic. If a miss is indicated, the checker causes a "replay" of the offending instruction, **using the copy of the instruction from the delay unit**. More specifically, Sager discloses that '[i]f a miss is indicated, the checker causes a "replay" of the offending instruction and any which depended on it or which were otherwise incorrect as a result of the erroneous data speculation. When the instruction was handed from the reservation station to the execution core, **a copy of it was forwarded to a delay unit** which provides a delay latency which matches the time the instruction will take to get through the execution core, TLB/TAG, and hit/miss units, so that the **copy** arrives at the checker at about the same time that the hit/miss logic tells the checker that the data speculation was incorrect." (Col. 9, lines 30-42, emphasis added). Applicants respectfully submit that the delay unit in Sager is not "a multiplexable data stream delayline for receiving said data stream", as claimed in Claim 1.

The device claimed in Claim 1, as amended, is for data stream analyzing. It enables parsing of the data stream in a way that is controlled by an interchangeable program. The device comprises a processor means, a program memory, and a multiplexable data stream delayline for receiving the data stream. Applicants respectfully submit that Sager does not teach or suggest

parsing a data stream or a multiplexable data stream line to enable such parsing.

For the above reasons, Applicants respectfully submit that Claim 1 is not obvious based on Baker, et al. or based on the combination of Baker, et al. and Sager. Claims 8-11 depend directly or indirectly from Claim 1 and would not be obvious for the same reasons as above for Claim 1.

Moreover, regarding Claim 8, the Examiner states that Baker, et al. discloses registers, and therefore, the Examiner rejects Claim 8 as being obvious based on Baker, et al. (See Col. 6, line 44). Applicants disagree. Applicants respectfully submit that Baker, et al. does not teach or suggest registers for operating on a datastream **before an actual comparison of the data with other data is executed**, as claimed in Claim 8. Therefore, Applicants respectfully submit that, for these additional reasons, Claim 8 is not obvious based on Baker, et al.

Response to Rejection of Claims 2-6 under 35 U.S.C. §103(a)

The Examiner has rejected Claims 2-6 under 35 U.S.C. 103(a) as being obvious based on Baker, et al. in view of Sager. The Examiner states that, although Baker, et al. does not disclose a multiplexable data stream delayline and multiplexing means for connecting different portions of data to the processor, Sager teaches these elements.

As discussed above, Baker, et al. in view of Sager does not teach or suggest the device having a multiplexable data stream delayline as claimed in Claim 1, as amended. Claims 2-6 depend directly or indirectly from Claim 1 and are respectfully submitted as being non-obvious for the same reasons stated above for Claim 1.

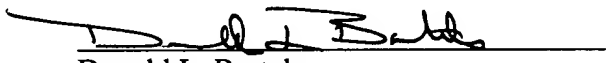
In addition, Sager discloses a multiplexor coupled to the input of the execution core which selects for execution among instructions from the delay unit and various other units according to a priority scheme. (See Col. 3, lines 54-67). Applicants respectfully submit that Sager does not teach or suggest having **different parts of the data stream** connected to the processor means via a multiplexing means, as claimed in Claim 2, as amended. For this additional reason, Applicants respectfully submit that Claim 2 is not obvious based on Baker, et al. and Sager. Claims 3-6 depend from Claim 2 and are respectfully submitted as not being obvious based on Baker, et al. and Sager for the same additional reasons as above for Claim 2.

Conclusion

For the above reasons, Applicants respectfully submit that all pending claims, Claims 1-11, in the present application are in condition for allowance. Such allowance is respectfully solicited.

If a telephone conference would expedite prosecution of this application, the Examiner is invited to telephone the undersigned at (650) 739-2800.

Respectfully submitted,



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